Design of an Evaluation Platform for an Analog-to-Digital Converter ASIC

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11.10.2013

Contents

Introduction

For the Projektseminar I designed, built and tested an evaluation platform for an ADC ASIC designed at the Fachbereich Integrierte Elektronische Systeme by MSc. Harish Balasubramaniam. The platform has to supply all necessary voltages, clock and control signals and breakout the signals that need to be measured. To be able to swap out broken parts and make the design reusable a modular approach has been implemented. The modules were arranged around a main board that carries the device under test (DUT).

High Level Design

Rationale

When a complex ASIC, after many months of simulating and tweaking, finally gets manufactured its performance has to be checked. Several measurements are made and the results compared to those from the simulations. Only then a verdict can be reached if the goals that were set for the design have been achieved. However, to conduct these measurements, support circuitry surrounding the device-under-test (DUT) is needed. For this seminar I went through the steps necessary to design this kind of circuits for a complex ASIC designed at the Fachgebiet Integrierte Elektronische Systeme. All circuits designed over the course of the seminar were specified in a way that they do not limit the performance of the DUT. The particular fitness of each module was verified through appropriate measurements.

Block Diagram

As can be seen in the block diagram, the main board is the center-piece of the system. It carries the DUT and breaks out supply voltages, additional voltages and I/O. It also includes the circuitry to drive the ADC's differential inputs with a single-ended signal coming from a function generator. It is itself connected to a Xilinx FPGA development board, which is used to generate the necessary digital control signals and read back the data. The two power-supply boards provide the core voltages for the ASIC. The DAC board generates twelve reference voltages needed for the ASIC's internal circuitry. Finally the clock board receives a reference clock from the FPGA board. This clock signal is converted from LVDS to LVCMOS levels.

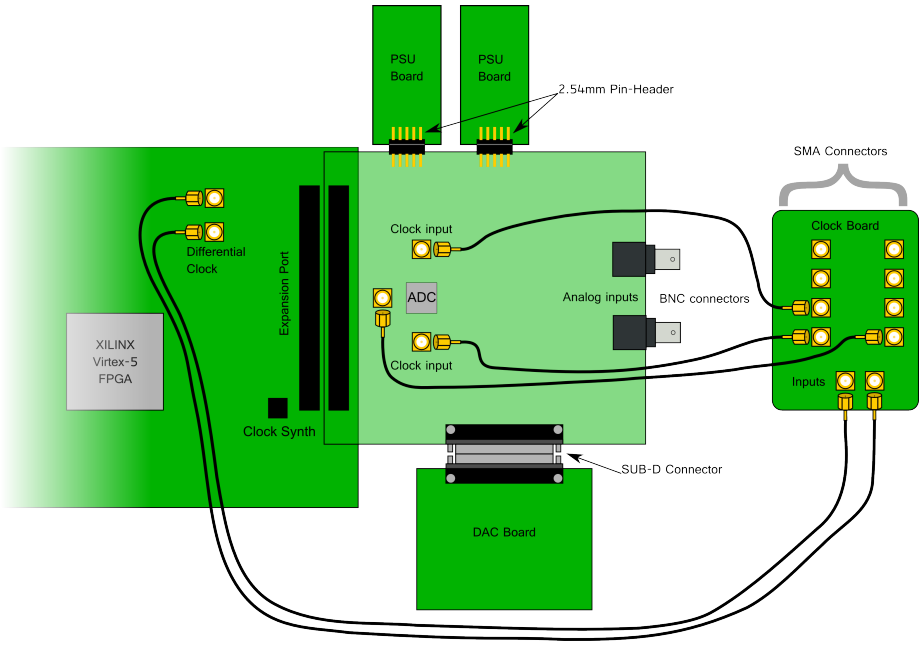
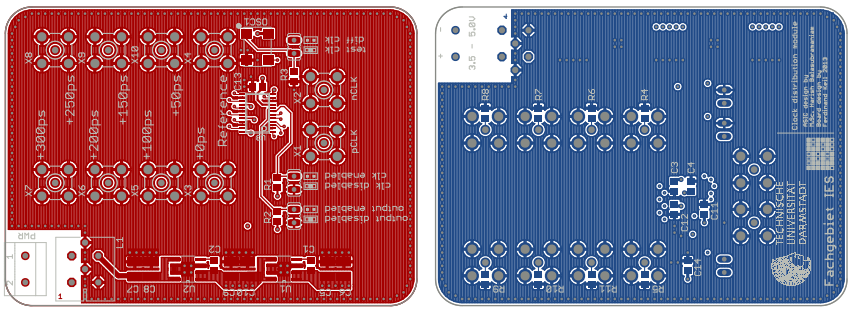


Figure 1: Block diagram

Modules

Clock Module



(a) Top side (b) Bottom side

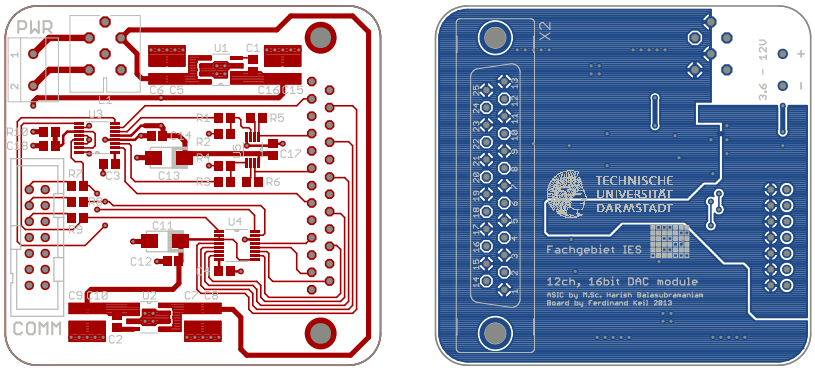
Figure 2: Clock module PCB layout (inner layers were omitted for clarity).

The clock board is based on the *ICS8308I*[1] by IDT. This clock fanout buffer

[1] http://www.idt.com/. . . /8308i-low-skew1-8-differentiallvcmos-lvcmos-fanout-buffer

offers eight low-jitter LVCMOS outputs and a differential as well as an LVCMOS input. It is specified up to 350 MHz. For maximum performance the necessary 3.3 V and 2.5 V rails are generated on-board. The board also includes an 80 MHz oscillator that can supply a test-clock to the LVCMOS input of the *ICS8308I*. The clock board also includes built-in delay lines ranging from 0 ps to 300 ps in 50 ps steps.

DAC Module



(a) Top side (b) Bottom side

Figure 3: DAC module PCB layout.

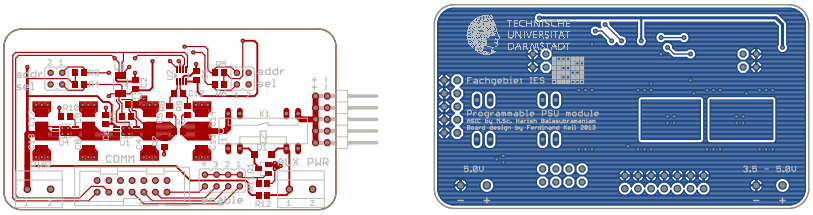
The DAC module outputs 12 precision reference voltages. These are generated by two I²C compatible 16-Bit digital-to-analog converters (DAC). The two DACs used on this board are the *AD5669*[2] and *AD5696*[3] from Analog Devices. These DACs come with an integrated reference voltage of 2.5 V for an output from 0 V to 2.5 V. Two of the *AD5696*' outputs are scaled to a range of 0 −1.0 V for an even higher resolution. A resistor voltage divider is used to scale the voltages and its output is buffered by an *ADA4528-2*[4] precision, ultralow noise OpAmp. For these outputs one LSB equals about 15 µV.

Particular attention was paid to the power supply design for the DAC board. Each DAC has its own dedicated *LT1763*[5] low noise linear regulator. The analog and logic supply pins of the *AD5696* are decoupled by an RC-filter to prevent logic noise coupling into the analog supply. Also a split ground plane was used, separating logic and analog ground.

[2] http://www.analog.com/. . . /ad5669r/products/product.html
[3] http://www.analog.com/. . . /ad5696r/products/product.html
[4] http://www.analog.com/. . . /ada4528-2/products/product.html
[5] http://www.linear.com/product/LT1763

The DAC module can be programmed via the I²C lines on its communication connector. The outputs are accessible through a shielded SUB-D 25-pin connector.

Power Supply Module



(a) Top side (b) Bottom side

Figure 4: Power supply module PCB layout.

The power supply module is based on the *LT3085*[6] by Linear Technology. The output voltage of this low dropout linear regulator can be programmed with just one resistor, making it easy to control it with a digital potentiometer. It also has low output noise of just 40 μV_{RMS} (10 Hz to 100 kHz). The digital potentiometer used is the *MCP4552-104E*[7] from Microchip, which is an I²C device. To control the output voltage and current the *INA219B*[8] was used, it can be read out trough I²C as well.

The input voltage first goes into a pre-regulator and is lowered to 1.82 V. After this regulator comes a programmable regulator, which is followed by a current shunt that is connected to the *INA219*. Finally a relay connects the output voltage to the header which plugs into the main board. The relay can be used to implement a specific power-up sequence for the DUT.

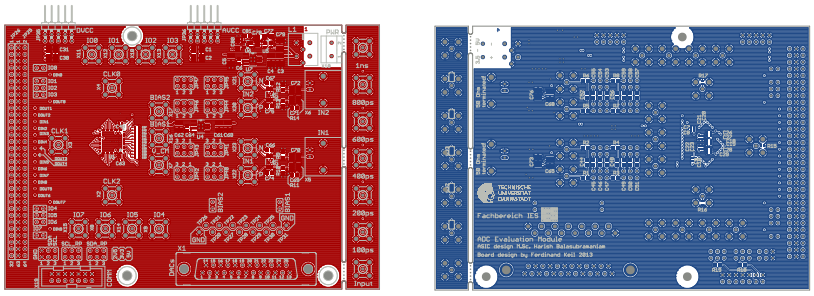
The communication connector on the power supply board is the same as the one on the DAC board, making it easy to connect all board together on one bus.

Main Board

The main board carries the device under test and connects to all the other modules as well as to the FPGA board. It also provides differential ADC input drivers and the 2.5 V I/O supply voltage.

Input signals for the board can be supplied as single-ended signals through two BNC connectors. On the board two *AD8476*[9] unity gain differential ADC drivers

[6] http://www.linear.com/product/LT3085
[7] http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en538371
[8] http://www.ti.com/product/ina219
[9] http://www.analog.com/.../ad8476/products/product.html



(a) Top side (b) Bottom side

Figure 5: Main board PCB layout (inner layers were omitted for clarity).

perform the single-ended to differential conversion. The common-mode voltage of these amplifiers is connected to the DAC module and thus programmable. To enable the signals to swing close to zero volts the amplifiers are supplied with ±2.5 V. The negative voltage is derived from the positive supply by an *LM2664*[10] charge-pump inverter and regulated by an *TPS72325*[11] negative linear regulator. The *AD8476*s are followed by a two-stage low-pass RC filter network. Their corner frequency can be changed through jumper settings.

As this is a mixed signal design, with precision DC voltages and high-frequency clock and data lines on the same board, a four layer PCB was used. The two outer layers carry as few signals as possible and were flooded with a ground plane. The ground plane acts as shield for the precision voltages and improves the signal integrity of the high-speed digital lines. Several critical signals were routed with matched trace lengths to ensure proper data transfer. All digital connections were placed on the left side of the board, all analog connections on the right. Digital and analog signals do not cross each other.

Using the communication connector on the main board the two PSU modules and the DAC module can be controlled from the FPGA board. This enables automated test setups.

Results

Clock module

The performance of the clock module was verified using a Tektronix TDS7404 4 GHz oscilloscope. The differential clock input was connected to the clock output of a Xilinx ML505 FPGA evaluation board. Unfortunately the output

[10] http://www.ti.com/product/lm2664
[11] http://www.ti.com/product/tps72325

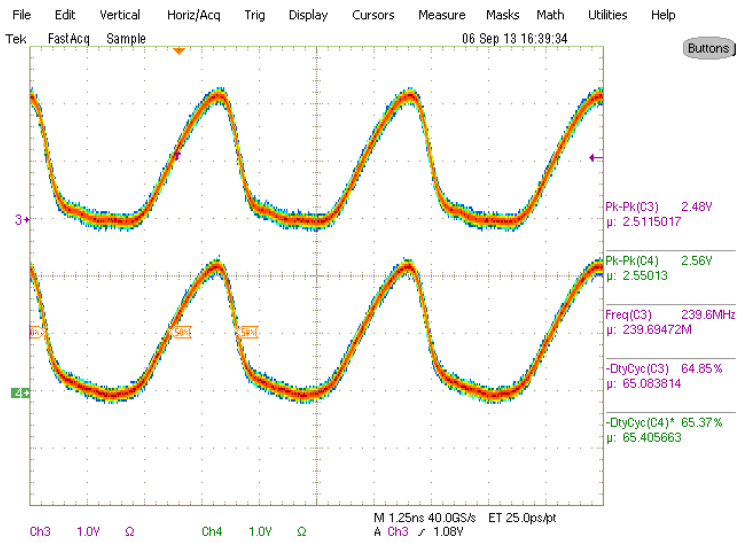


Figure 6: Screenshot of with one output of the clock module directly connected to TDS7404 input (50 Ω terminated).

signals from the clock module are far from a square wave (see Figure 6). The possible causes for these signal integrity issues include ground bounce, insufficient decoupling and impedance mismatch. The root cause however could not be identified.

The actual delay times were measured using the TDS7404 oscilloscope, the values are shown in Table 1.

Calculated delay [ps]	**Measured delay [ps]**	**Error [ps]**	
0	36.08	36.08	-
50	66.76	16.76	33.52%
100	96.00	4.00	4.00%
150	164.05	14.05	9.37%
200	214.63	14.63	7.32%
250	272.50	22.50	9.00%
300	316.92	16.92	5.64%

Table 1: Measurement results for the delay-lines on the clock board.

DAC module

The resolution and accuracy of the DAC outputs were verified using a calibrated Hameg HM8112-2 6.5-digit multimeter. Multiple measurements were taken to check for linearity and offset. Also the noise was measured with an oscilloscope, however it was below the noise floor of the available unit.

Power Supply Module

The power supply board has been tested at its maximum specified output current of 500 mA over the full output voltage range from 0.5 V to 1.5 V. Under load the temperature of the pre-regulator - which is producing the most heat - reached 100°°C and thus stayed well below the maximum allowable temperature of 125°°C for the *LT3085*. The *INA219B* current shunt IC was tested successfully as well. The values measured by it were verified using the Hameg HM8112-2 multimeter.

The output noise of the circuit was below the noise floor of the available equipment.

Main Board

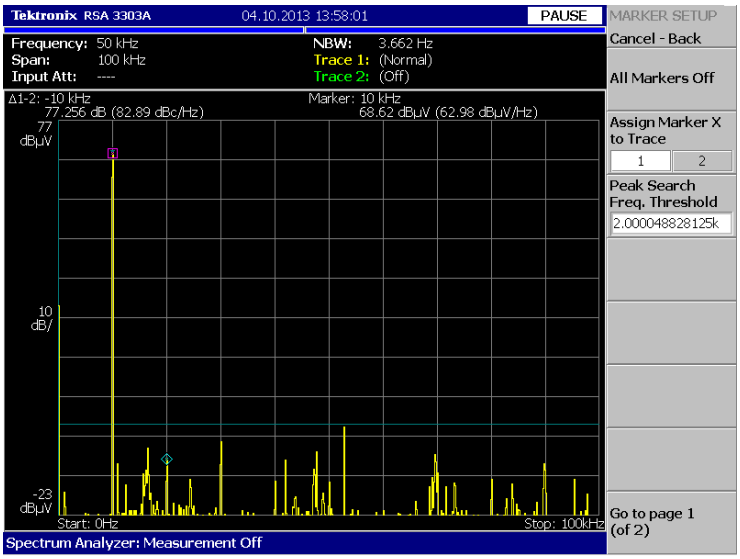


Figure 7: Output spectrum of the ADC driver on the main board (captured with Tektronix RSA3303).

For the main board the performance of the ADC driver was of interest. First of all the phase shift between the positive and negative differential outputs was

measured using a Hameg HM8123 programmable counter. It was found to be between 178.0° to 180.5° for frequencies from 1 kHz and 22 kHz.

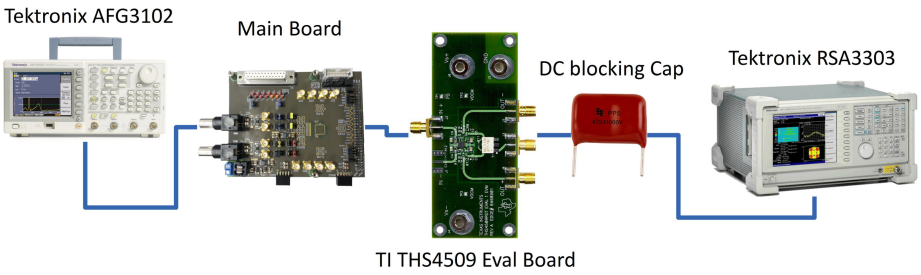


Figure 8: Measurement setup for the distortion measurement.

The most important characteristic for the ADC driver however is the harmonic distortion and noise. For the measurement the Tektronix AFG3102 arbitrary waveform generator was used as a signal source, a TI THS4509 OpAmp evaluation board as buffer and the Tektronix RSA3303 spectrum analyzer for the actual measurement. The setup is illustrated in Figure 8. The resulting output spectrum can be seen in Figure 7. As the spectrum clearly shows the output noise of the *AD8476* is below the detectable threshold for most frequencies. The second harmonic is about 80 dB below the fundamental. The actual value is most likely even better, however it could not be measured as for the limitations of the setup.

Conclusions

With the notable exception of the clock module the designed evaluation platform met its requirements. As of October 11th, 2013 it is used by MSc. Harish Balasubramaniam in the testing of his ADC chip. Preliminary tests are promising and all modules seem to be up to the task.

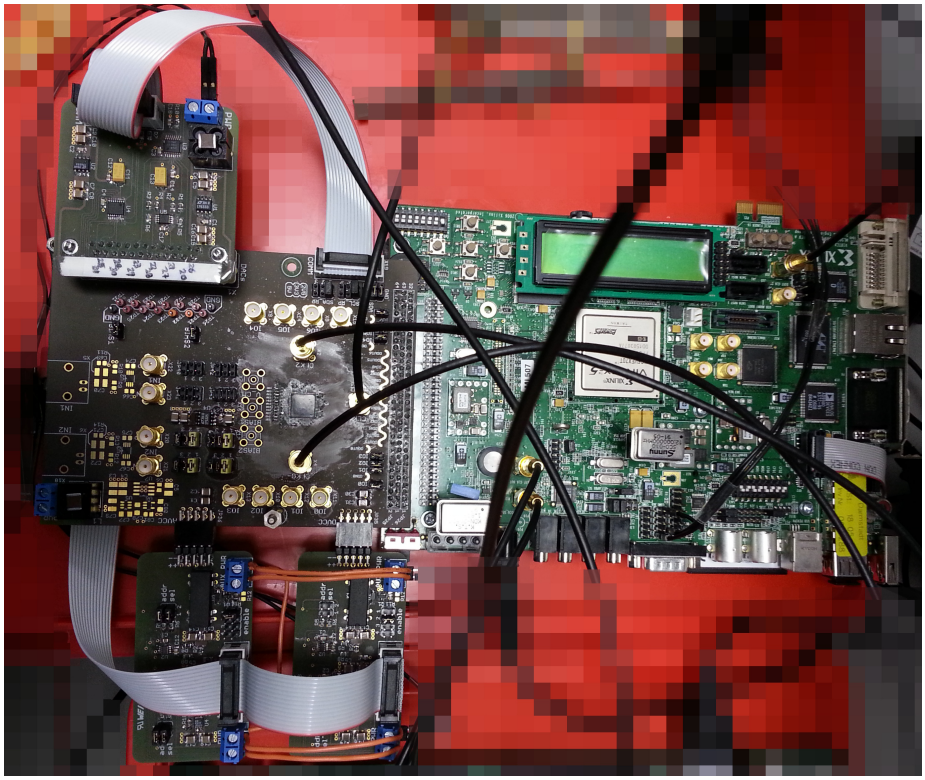
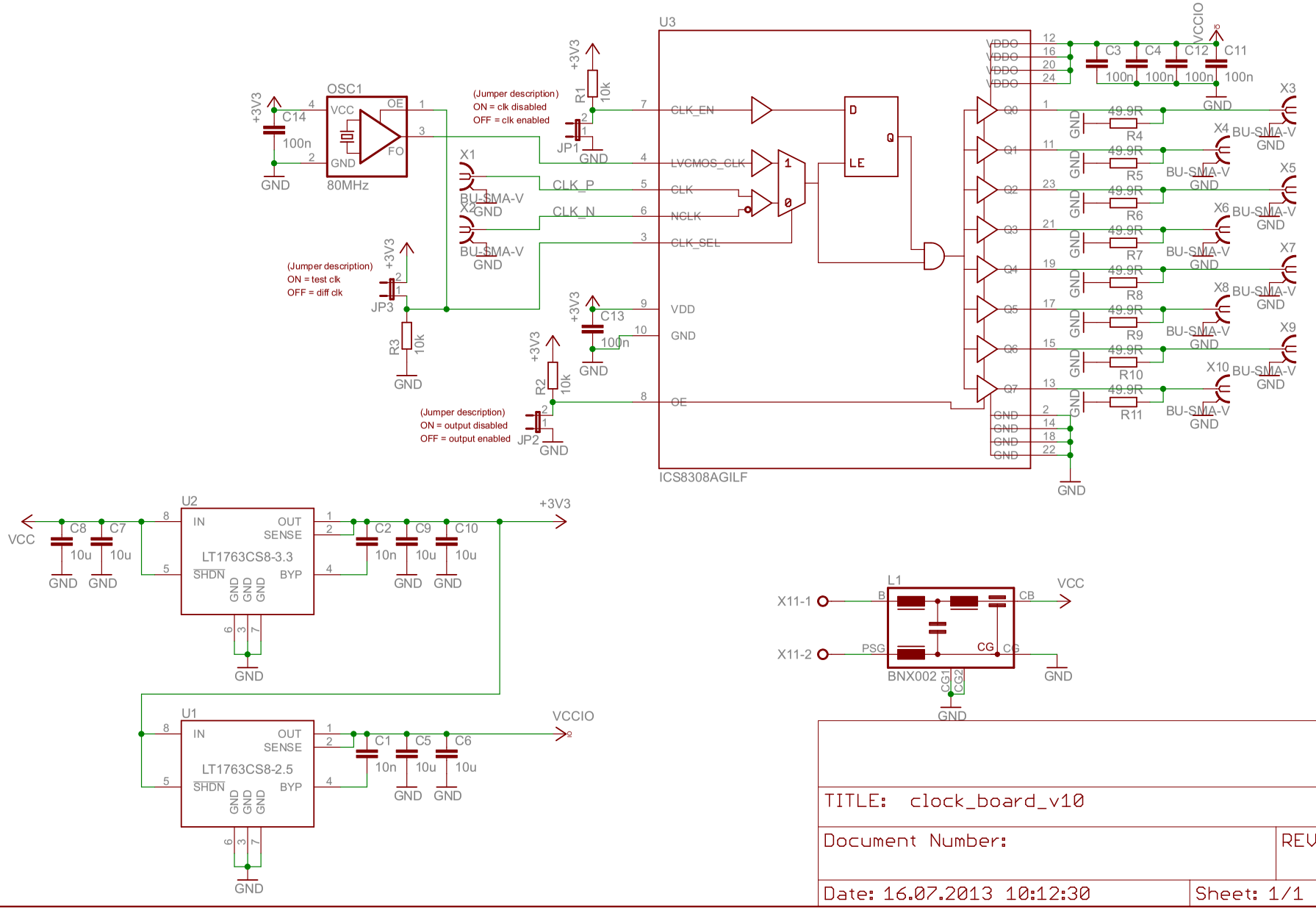


Figure 9: Final test setup.

Appendices

Clock Module Schematic (v10)


U3
ICS8308AGILF
OSC1
80MHz
C14
100n
R1
10k
JP1
(Jumper description)
ON = clk disabled
OFF = clk enabled
X1
X2
BU-SMA-V
CLK_P
CLK_N
CLK_EN
LVCMOS_CLK
CLK
NCLK
CLK_SEL
VDD
GND
OE
(Jumper description)
ON = test clk
OFF = diff clk
JP3
R3
C13
R2
(Jumper description)
ON = output disabled
OFF = output enabled
JP2
D
Q
LE
VDDO
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
C3
C4
C12
C11
VCCIO
49.9R
R4
R5
R6
R7
R8
R9
R10
R11
X3
X4
X5
X6
X7
X8
X9
X10
U2
LT1763CS8-3.3
IN
OUT
SENSE
SHDN
BYP
C8
C7
C2
C9
C10
10u
10n
VCC
+3V3
U1
LT1763CS8-2.5
C1
C5
C6
L1
BNX002
X11-1
X11-2
CB
CG
PSG
CG1
CG2
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Document Number:
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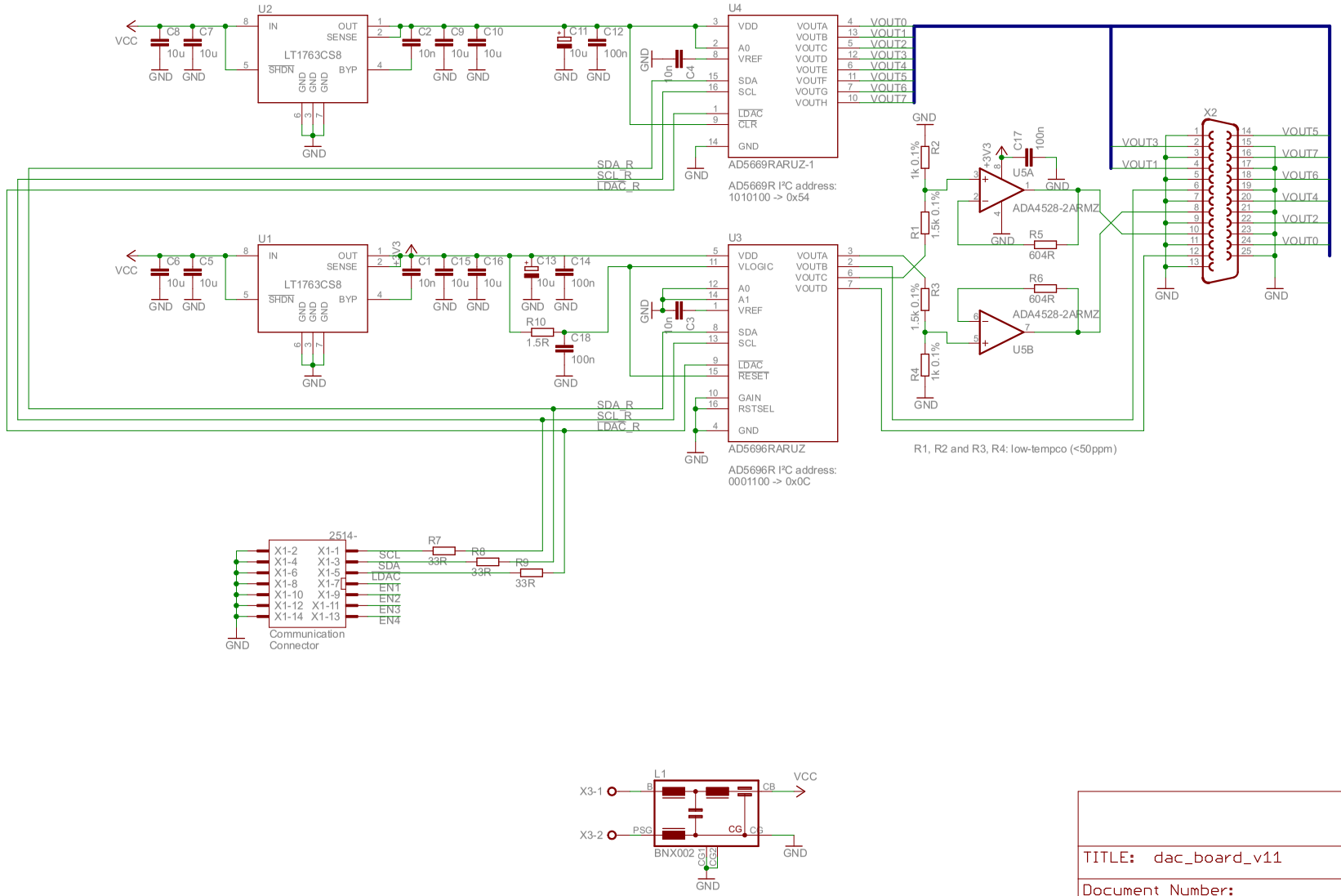
Date: 16.07.2013 10:12:30
Sheet: 1/1

DAC Module Schematic (v11)



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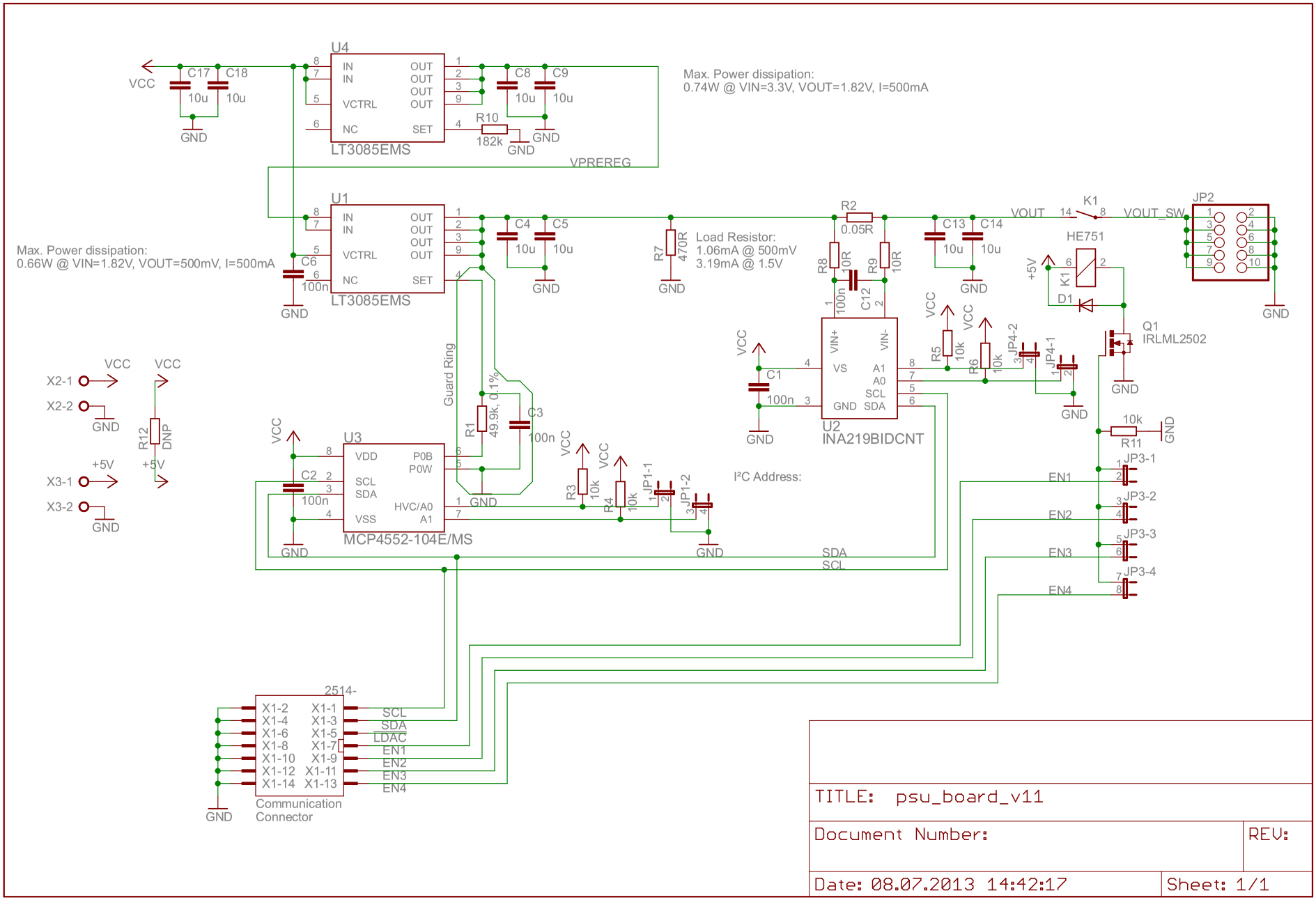
Power Supply Module Schematic (v11)


U4
LT3085EMS
C17
C18
10u
10u
GND
VCC
C8
C9
R10
182k
VPREREG
Max. Power dissipation:
0.74W @ VIN=3.3V, VOUT=1.82V, I=500mA
U1
LT3085EMS
C6
100n
C4
C5
R7
470R
Load Resistor:
1.06mA @ 500mV
3.19mA @ 1.5V
Max. Power dissipation:
0.66W @ VIN=1.82V, VOUT=500mV, I=500mA
R2
0.05R
R8
10R
R9
10R
C12
100n
C13
C14
VOUT
K1
HE751
D1
VOUT_SW
JP2
Q1
IRLML2502
U2
INA219BIDCNT
C1
100n
R5
10k
R6
10k
JP4-1
JP4-2
R11
10k
X2-1
X2-2
X3-1
X3-2
R12
DNP
U3
MCP4552-104E/MS
C2
100n
R1
49.9k, 0.1%
C3
100n
Guard Ring
R3
10k
R4
10k
JP1-1
JP1-2
I²C Address:
JP3-1
JP3-2
JP3-3
JP3-4
EN1
EN2
EN3
EN4
SDA
SCL
2514-
X1-2
X1-4
X1-6
X1-8
X1-10
X1-12
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X1-3
X1-5
X1-7
X1-9
X1-11
X1-13
LDAC
Communication
Connector
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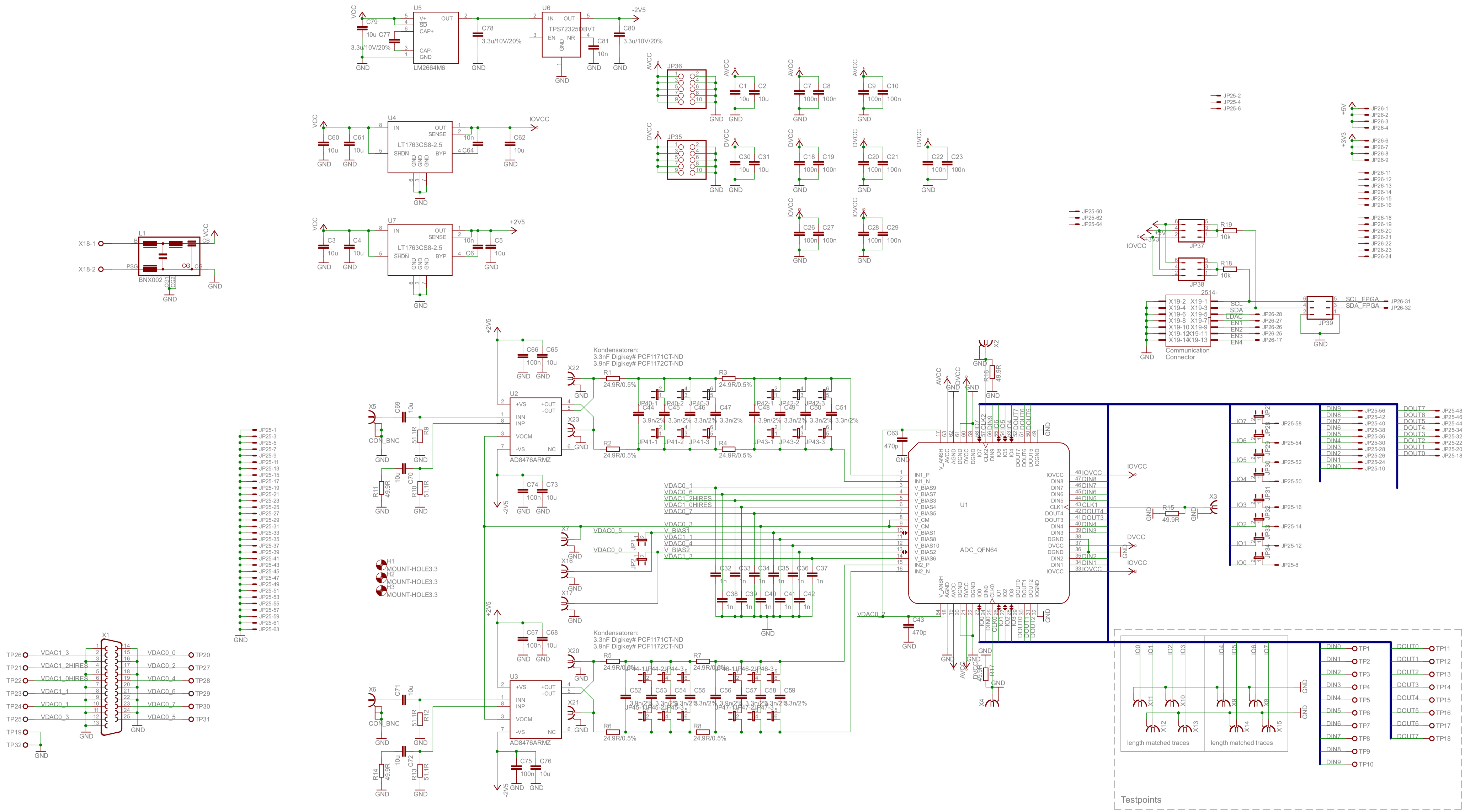
Sheet: 1/1

Main Board Schematic (v10)

Note: The values for R1-R8 and C44-C59 have been changed.


U5
LM2664M6
U6
TPS72325DBVT
U4
LT1763CS8-2.5
U7
LT1763CS8-2.5
L1
BNX002
JP36
JP35
U2
AD8476ARMZ
U3
AD8476ARMZ
Kondensatoren:
3.3nF Digikey# PCF1171CT-ND
3.9nF Digikey# PCF1172CT-ND
U1
ADC_QFN64
X1
MOUNT-HOLE3.3
Communication
Connector
JP37
JP38
JP39
SCL_FPGA
SDA_FPGA
length matched traces
Testpoints
CON_BNC
VCC
AVCC
DVCC
IOVCC
+2V5
-2V5
+5V
+3V3
GND